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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/733,418	12/08/2000	Salman Akram	96-0841.01	6082

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EXAMINER	
BROCK II, PAUL E	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 07/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/733,418	AKRAM, SALMAN	
	Examiner	Art Unit	
	Paul E Brock II	2815	

-- The MAILING DATE of this communication app ars on the cover sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *57-65* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *57-65* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 57 – 65 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. It is not clear where in the originally filed specification support for "forming a second trench into the semiconductor substrate at the bottom of the first trench using the spacers as an etching guide, wherein an overall depth of the first and second trenches is two times a depth of a bordering diffusion region determined by an area containing at least approximately 90% concentration of conductive atoms;" can be found. While the originally filed specification provides support for forming "area containing at least approximately 90% concentration of conductive atoms" after forming a second trench and forming an insulative material in first and second trenches, no support exists for the overall depth of the first and second trenches being defined by "an area containing at least approximately 90% concentration of conductive atoms" during the formation of the second trench.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 57 – 65 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. The term "at least approximately 90%" in claims, 57, 60, and 63 is a relative term which renders the claim indefinite. The term "at least approximately 90%" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. What is concentration of conductive ions that define the diffusion region? Any range or example of what is encompassed by "at least approximately 90%" is not defined in the specification.

6. Claim 60 recites the limitation "the single oxide layer" in the sixth line of the claim. There is insufficient antecedent basis for this limitation in the claim. For purposes of this office action "forming a single semiconductive layer lining a surface of the first trench" in line four of the claim will be considered -- forming a single oxide layer lining a surface of the first trench --, and "the single semiconductive layer" in the last two lines of the claim will be considered -- the single oxide layer --.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 57 – 65 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu (USPAT 5393692) in view of Kameyama (USPAT 4472240).

With regard to claim 57, Wu discloses in figures 8 – 11b a process for forming device isolation for a semiconductor assembly. Wu discloses in figure 9 forming a first trench (54) having sidewalls into a semiconductor substrate (20). Wu discloses in figure 10 forming a single oxidizable layer (55) lining on a surface of the first trench. It should be noted that the oxide layer 55 of Wu is an oxidizable layer. Wu discloses in figure 11 forming spacers (58) of oxidizable material (polysilicon) along the sidewalls of the first trench over and in direct contact with the single oxidizable layer. Wu discloses in figures 11 – 11a forming an insulative material (63) in the first trench at least partially by substantially consuming the oxidizable material of the spacer and the single oxidizable layer. Wu does not disclose forming a second trench into the semiconductor substrate at the bottom of the first trench using the spacers as an etching guide. Kameyama teaches in figure 4e forming a second trench (107) into a semiconductor substrate (101) at the bottom of a first trench (104) by using spacers (106a and 106b) as an etching guide. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the etching of the second trench of Kameyama in the method of Wu in order to form an

element isolation region in a self-aligned manner with excellent controllability without forming a cavity therein as stated by Kameyama in column 2, lines 51 – 55. It would have been further obvious in the method of Wu and Kameyama that the step of forming the insulative material comprises forming the insulative material in the first and second trenches at least partially by substantially consuming the oxidizable material of the spacer and the single oxidizable layer. As far as the examiner can ascertain, Wu and Kameyama teach wherein an overall depth of the first and second trenches is two times a depth of a bordering diffusion region determined by an area containing at least approximately 90% concentration of conductive atoms in the step of forming the second trench.

With regard to claim 60, Wu discloses in figures 8 – 11b a process for forming device isolation for a semiconductor assembly. Wu discloses in figure 9 forming a first trench (54) having sidewalls into a semiconductor substrate (20). Wu discloses in figure 10 forming a single oxide layer (55) lining on a surface of the first trench. Wu discloses in figure 11 forming spacers (58) of semiconductive material (polysilicon) along the sidewalls of the first trench over and in direct contact with the single oxide layer. Wu discloses in Wu discloses in figures 11 – 11a forming an insulative material (63) in the first trench at least partially by substantially consuming the semiconductive material of the spacer and the single oxide layer. Wu does not disclose forming a second trench into the semiconductor substrate at the bottom of the first trench using the spacers as an etching guide. Kameyama teaches in figure 4e forming a second trench (107) into a semiconductor substrate (101) at the bottom of a first trench (104) by using spacers (106a and 106b) as an etching guide. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the etching of the second trench of Kameyama in the

method of Wu in order to form an element isolation region in a self-aligned manner with excellent controllability without forming a cavity therein as stated by Kameyama in column 2, lines 51 – 55. It would have been further obvious in the method of Wu and Kameyama that the step of forming the insulative material comprises forming the insulative material in the first and second trenches at least partially by substantially consuming the semiconductive material of the spacer and the single oxide layer. As far as the examiner can ascertain, Wu and Kameyama teach wherein an overall depth of the first and second trenches is two times a depth of a bordering diffusion region determined by an area containing at least approximately 90% concentration of conductive atoms in the step of forming the second trench.

With regard to claim 63, Wu discloses in figures 8 – 11b a process for forming device isolation for a semiconductor assembly. Wu discloses in figure 9 forming a first trench (54) having sidewalls into a semiconductor substrate (20). Wu discloses in figure 10 forming a single oxide layer (55) lining on a surface of the first trench. Wu discloses in figure 11 forming spacers (58) of silicon material (polysilicon) along the sidewalls of the first trench over and in direct contact with the single oxide layer. Wu discloses in Wu discloses in figures 11 – 11a forming an oxide filler (63) in the first trench at least partially by substantially consuming the silicon material of the spacer and the single oxide layer. Wu does not disclose forming a second trench into the semiconductor substrate at the bottom of the first trench using the spacers as an etching guide. Kameyama teaches in figure 4e forming a second trench (107) into a semiconductor substrate (101) at the bottom of a first trench (104) by using spacers (106a and 106b) as an etching guide. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the etching of the second trench of Kameyama in the method of Wu in

order to form an element isolation region in a self-aligned manner with excellent controllability without forming a cavity therein as stated by Kameyama in column 2, lines 51 – 55. It would have been further obvious in the method of Wu and Kameyama that the step of forming the insulative material comprises forming the oxide filler material in the first and second trenches at least partially by substantially consuming the silicon material of the spacer and the single oxide layer. As far as the examiner can ascertain, Wu and Kameyama teach wherein an overall depth of the first and second trenches is two times a depth of a bordering diffusion region determined by an area containing at least approximately 90% concentration of conductive atoms in the step of forming the second trench. Wu discloses in figures 11b planarizing the oxide filler.

With regard to claims 58, 61, and 64, Wu discloses in figures 11 – 11a and column 5, line 66 – column 6, line 9 wherein forming the insulative material (oxide filler) comprises annealing the semiconductor assembly in the presence of an oxidizing agent.

With regard to claim 59, 62, and 65, Wu discloses in figures 8 – 11b wherein the process uses only one mask (28) to form the device isolation.

Response to Arguments

7. Applicant's arguments have been considered but are moot in view of the new claims and the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (571) 272-1723. The examiner can normally be reached on 8:30 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul E Brock II